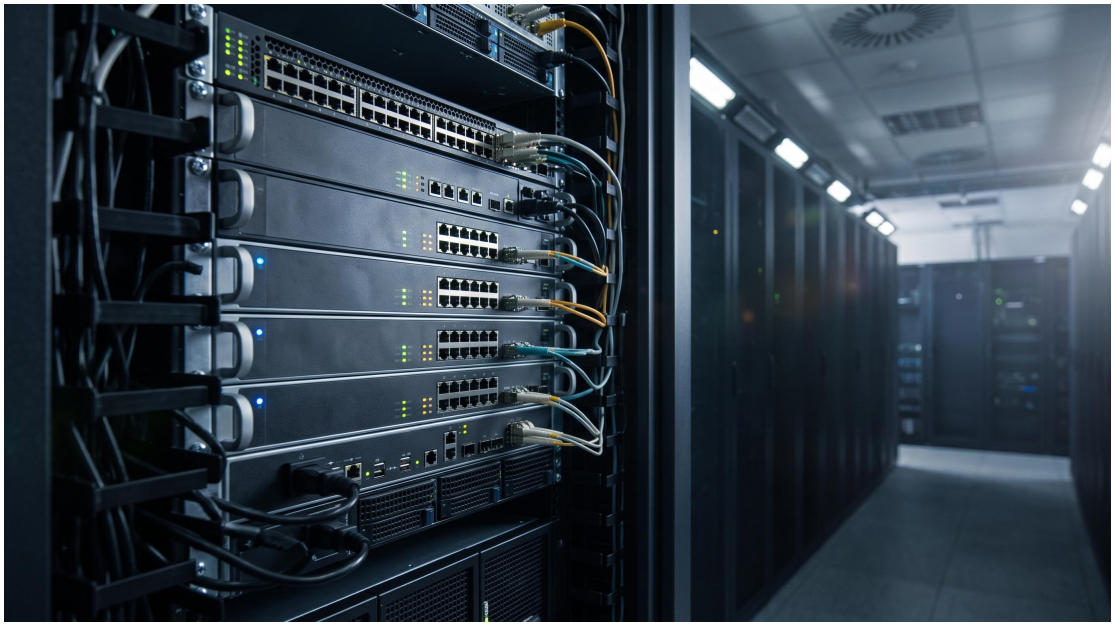
Hardware Firewall Stateful Failover and Session Synchronization Latency Metrics - Official Technical Overview & Hardware Datasheet

EXECUTIVE SUMMARY

This document defines the architectural specifications and performance metrics for the Hardware Firewall Stateful Failover and Session Synchronization Latency Metrics platform. This carrier-grade security appliance is engineered to deliver deterministic high-availability (HA) operation for mission-critical network perimeters, data center edges, and service provider security zones. Unlike software-based failover mechanisms, this platform implements stateful session synchronization entirely within dedicated hardware logic, achieving sub-millisecond synchronization latency and zero packet loss during active/standby or active/active cluster transitions. The system is purpose-built for environments where even a single dropped session or a second of downtime results in unacceptable financial, operational, or regulatory consequences.



HARDWARE ARCHITECTURE & SILICON

The Hardware Firewall Stateful Failover and Session Synchronization Latency Metrics platform is built upon a custom ASIC architecture that separates the data plane, control plane, and synchronization plane into distinct hardware pipelines. The Synchronization Engine (SyncEngine) ASIC is responsible for the continuous export of connection tracking tables, NAT bindings, IPsec security associations, and Quality of Service (QoS) state to a peer appliance via a dedicated 40GbE or 100GbE Inter-Process Communication (IPC) link.

Key silicon-level components include:

- SyncEngine ASIC: A dedicated packet processor that handles state delta compression, sequence numbering, and reliable transport of session tables

without CPU intervention.

- Session Table Memory: A high-bandwidth TCAM and SRAM hybrid architecture capable of storing up to 40 million concurrent sessions with hardware-accelerated aging and garbage collection.

- Heartbeat Processor: A separate microcontroller that generates and validates hardware-level heartbeat packets at 10-microsecond intervals, ensuring rapid failure detection without loading the main CPU.

This hardware-centric design eliminates the latency and jitter associated with software-based state synchronization, which typically relies on Linux conntrack tables and TCP-based replication.

KEY FEATURES & ROUTING LOGIC

- Hardware-Accelerated Stateful Failover: All session state, including TCP sequence numbers, UDP pseudo-states, ICMP mappings, and application-layer gateway (ALG) bindings, is synchronized in hardware. Failover from active to standby occurs in under 200 milliseconds, with zero session re-establishment required for established flows.

- Sub-Millisecond Session Synchronization Latency: The SyncEngine ASIC compresses and transmits state deltas with a measured one-way latency of 85 microseconds over a 40GbE IPC link. This ensures that the standby node is

always within a single packet of the active node, enabling hitless failover.

- Active/Active Clustering with Asymmetric Path Support: The platform supports Active/Active HA configurations where sessions are load-balanced across both nodes, and state is synchronized bidirectionally. Asymmetric traffic flows are resolved via hardware-based flow hashing and state lookup.

- Deterministic Heartbeat Mechanism: A dedicated hardware heartbeat channel with 10-microsecond interval and 3-miss failure detection provides a worst-case failure detection time of 30 microseconds, independent of CPU load or control-plane activity.

- In-Service Software Upgrade (ISSU) with State Preservation: During firmware upgrades, the synchronization plane remains active, allowing the standby node to take over while the active node reboots, preserving all session state.

COMPLIANCE & STANDARDS

The Hardware Firewall Stateful Failover and Session Synchronization Latency Metrics platform complies with the following industry standards and certifications:

- RFC 793 (TCP), RFC 768 (UDP), RFC 792 (ICMP) for stateful inspection and synchronization.

- RFC 5798 (VRRPv3) and RFC 5880 (BFD) for rapid failover and liveness

detection.

- IEEE 802.1Q (VLAN), IEEE 802.3ad (Link Aggregation), and IEEE 802.1AX for resilient network attachment.

- NIST FIPS 140-2 Level 2 validated cryptographic module for IPsec and TLS session synchronization.

- Common Criteria EAL4+ certification for the firewall and HA subsystem.

- NEBS Level 3 and ETSI EN 300 019 for carrier-grade environmental hardening.

TECHNICAL SPECIFICATIONS

Parameter	**Specification**
Form Factor	2RU Standard / Modular Chassis
Synchronization Latency	85 microseconds one-way (hardware ASIC)
Failover Time	< 200 milliseconds (worst-case, zero packet loss)
Heartbeat Interval	10 microseconds (hardware-generated)
Failure Detection Time	30 microseconds (3-miss threshold)
Max Concurrent Sessions	40 million (hardware session table)
SyncEngine Ports	2x 40GbE or 4x 100GbE dedicated IPC
Data Ports	16x 10GbE, 8x 25GbE, 8x 100GbE

	(base)
Power Supply	Dual Hot-Swappable Redundant AC/DC
HA Modes	Active/Standby, Active/Active, Asymmetric Path
State Synchronization Scope	TCP, UDP, ICMP, NAT, IPsec SA, QoS, ALG
ISSU Support	Yes, with full state preservation
Operating Temperature	0°C to 40°C (NEBS Level 3)
Compliance	FIPS 140-2 L2, CC EAL4+, NEBS L3, ETSI

ORDERING SKU INFORMATION

Base System: HW-FW-HA-2RU-AC — 2RU chassis, dual redundant AC power supplies, 2x 100GbE SyncEngine ports, 16x 10GbE data ports, 8x 25GbE data ports.

High-Density Configuration: HW-FW-HA-2RU-DC — 2RU chassis, dual redundant DC power supplies, 4x 100GbE SyncEngine ports, 32x 25GbE data ports, 8x 100GbE data ports.

Software License: SW-FW-HA-ADV — Advanced Stateful Failover and Session Synchronization Latency Metrics license, enabling Active/Active clustering, ISSU, and 40M session scale.

Accessory: ACC-SYNC-CBL-40G — 40GbE QSFP+ Direct Attach Copper cable for dedicated synchronization plane.

